DC OFFSET CANCELLATION IN A DIRECT-CONVERSION RECEIVER

BACKGROUND OF THE INVENTION

Field of the Invention:

The present invention relates in general to direct-conversion receivers, or zero intermediate frequency (ZIF) receivers, in particular to circuit for canceling dc offset in such receivers.

Brief Description of Related Art

From the handbook "The ARRL Handbook For Radio Amateurs", Published by the American Radio Relay League, sixty-eight edition, 1991, the direct-conversion receiver (zero IF) was made known and has received a great deal of interest over the past few years by significantly improving on-chip integration. In a direct-conversion receiver, dc offset from RF front end and baseband (BB) can be amplified by many gain stages and thus may saturate the receiver at certain node depending on the amplitude of dc offset and the gain in the case. Even if the dc offset does not saturate the receiver, it can still cause malfunction when the dc offset is very close to the signal level. Therefore effective canceling the dc offset in the receiver is necessary. In U.S. Pat. No. 6,509,777, a programmable gain amplifier in series with a transconductance (gm) amplifier is placed in the feedback path, as shown in Fig. 1, to form a highpass filtering (HPF) function with variable cutoff frequencies. In U.S. Pat. No. 6,442,380, a passive HPF combined by a capacitor and a variable resistor to form variable cutoff frequencies is placed in several places in signal path in a ZIF receiver, as shown in Fig. 2.

SUMMARY OF THE INVENTION

An object of this invention is to optimize the trade off between the silicon area and power consumption for dc offset cancellation (DCOC) in a ZIF receiver. This invention can save large ratio of silicon area by reducing the integrator capacitor value used in conjunction with an integrator opamp by a factor of 3 to 4. The power consumed by the integrator opamp in today's deep submicron (DSM) and very deep submicron (VDSM) technologies can be very minor. Thus the use of the integrator does not increase much power in comparison with the use of a passive high-pass filter (HPF) for DC offset cancellation in U.S. Pat. No. 6,442,380. This invention uses active opamp integrator plus input current summing feedback which allows more leeway in choosing smaller integrating capacitor value and less power consumption comparing to U.S. Pat. No. 6,509,777 which used transconductor and output current summing feedback topology. This invention uses a

continuous time active integrator to realize low-pass filter (LPF), while in U.S. Pat. No. 6,509,777, the DC offset reduction circuit used switched-capacitor RC LPF which needs a clock signal to control the switch and increases the circuit complexity. The clock generator was not shown there but was necessarily used. This invention has the feature that the integrator opamp is easily realized to have very high DC gain and very large output swing, moderate bandwidth and small power consumption in modern DSM/VDSM technologies, and thus can provide a very large DC attenuation to achieve superior DC offset reduction. The resulted DC offset is very small compared to the signal and thus can be considered as being canceled.

In this invention, a feedback loop type HPF function is implemented with an active opamp integrator and voltage-to-current conversion (VIC) resistor driven by the integrator. The cutoff frequency is made variable by varying the input resistor in the integrator and the output VIC resistor. Any opamp used in the signal path in the receiver can be used as a summing point for the DCOC input and output signal.

The opamp can be designed for low power and providing rail to rail output voltage swing. This large output swing makes the design robust against larger DC offset to accumulate in a ZIF receiver [to accumulate] before it is cancelled by the DCOC block. This means designer can use fewer DCOC blocks in the receiver. This will reduce the silicon area and save power too.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig.1 shows a block diagram of a ZIF receiver analog front end commonly used nowadays in wireless communication systems. The base-band (BB) analog to digital converter (ADC) and digital signal processing (DSP) block are not shown. RF signal is received by the antenna and filtered by a RF bandpass (BPF) filter. Then the signal is amplified by the low noise amplifier (LNA) and directly down-converts from RF to BB by mixing with the local oscillator (LO) signal in the mixer. The signal is then filtered again by a lowpass filter (LPF). The amplitude of the signal is controlled by digital automatic gain control (AGC) system and amplified by a variable gain amplifier (VGA). The signal is passed to BB DSP portion by BB driver. A DCOC scheme can be used in this ZIF receiver at any point in signal path from BB LPF to BB driver, provided that at that point there is an opamp in signal path which will be used as summing point.

Fig.2 shows a DCOC circuit in U.S. Pat. No. 6,509,777.

Fig.3 shows a DCOC circuit in U.S. Pat. No. 6,442,380.

Fig.4 shows a DCOC circuit in present invention.

Fig.5 shows how the present invention circuit is used in a ZIF receiver.

Fig.6 shows the simulation result of the DCOC effect.

DETAILED DESCRIPTION OF THE INVENTION

Fig.4 shows the DC offset cancellation block (DCOC) of the present invention. The circuit is used to feed back the integrated component from the output of a base-band amplifier of a ZIP receiver to a preceding stage. By negative feedback of the integrated component, the DC offset offset is minimized. The DCOC block comprises an OPAMP connected as an integrator or active low pass filter. The integrator has a feedback capacitor C1 connected between the inverting input and the non-inverting output, and another capacitor C1 connected between the non-inverting input and the inverting output. Each input is connected to a differential input voltage Vin through a resistor R1. R1 is variable to change the cutoff frequency of the low pass filter. The output voltage Vout of the integrator is connected to a virtual ground through a resistor R2 to flow an output current io equal to Vout/R2. Thus Vout is converted into i_{on}, and R2 constitutes a voltage-to-current converter VIC.

The DCOC is connected as a feedback block to a current summing stage of the base-band amplifier as shown in Fig.5. The stage includes an opamp OPAMP2 connected as an active low pass filter. A parallel R4 and C2 is connected between the inverting input and the non-inverting output, and another parallel R4 and C2 is connected between the non-inverting input and the inverting output. Each input is fed with a signal Vin through resistor R3 as input signal current, which is summed with the feedback current from the DCOC block. The output voltage Vout of OPAMP2 is then proportional to the sum of the signal voltage and the feedback voltage from the DCOC block.

The DCOC circuit can be applied to both the in phase component I path and the quadrature component Q path of a ZIF receiver. The integrated voltage is transferred into current by VIC resistor and fed back to the input of the opamp OPAMP2 in signal path. The cutoff frequency is therefore determined by four factors: integrator resistor R1, capacitor C2, opamp OPAMP1, and VIC resistor R2, and OPAMP2 feedback resistor R_4. A small increase in R_1/R_4 ratio can result a large reduction of the integrator capacitor value. In a ZIF receiver, the HPF cutoff frequency in signal path must maintain at a very low level so that the signal bandwidth degradation can be kept in minimum. To have this feature, the integrator capacitor and resistor need to have very large value to provide a large time constant. For example, a 1MΩresistor and 150pF capacitor form the time constant which

results a cutoff frequency around 1KHz. The presence of VIC resistor can contribute to the time constant linearly. As shown in Fig.5, if $R_4 = 5K\Omega$, $R_2 = 20K\Omega$, to achieve 1KHz cutoff frequency, then $C_1 = 37.5pF$. The silicon area for R_4 and R_2 can be easily less than $100um^2$, but for $C_1 = 150pF$, it can be as large as $135{,}000um^2$, because C_1 is a floating metal-metal capacitor. It is obvious that the use of VIC R_2 saves about 75% silicon area. Because R_2 contrubutes to the time constant, the mentioned feature to save silicon area applies to reduce integrating resistor value, R_1 in Fig.5, in another case where a small C_1 and a large R_1 are chosen for 1KHz cutoff frequency, for example, from original $R_1 = 10M\Omega$, $C_1 = 15pF$, shrinking to $R_1 = 2.5M\Omega$, $C_1 = 15pF$. The silicon area is also saved about 75%. If $R_1 = 10M\Omega$ is kept, the cutoff frequency is now set to 250Hz. The receiver performance [will] improves because less signal bandwidth is sacrificed. In a word, the invention can either cut the chip cost by [largely] saving silicon area, or improve the chip performance. It is a flexibility for right decision to make by a chip designer.

The DCOC circuit itself used in the present invention has a lowpass filtering function. From Fig.4, the transfer function can be simplified as:

$$H(s) = \frac{v_o}{v_{in}} = -\frac{A(s)}{1 + s(1 + A(s))R_1C_1}$$

where v_o is the output voltage, v_{in} is the input voltage, R_1 is the integrating resistance, C_1 is the integrating capacitance, and the opamp OPAMP1 is assumed to have a gain of $A(s)$. When OPAMP1 becomes ideal, the transfer function becomes ideal integrator function:

$$H_{ideal}(s) = \frac{v_o}{v_{in}} = -\frac{1}{sR_1C_1}$$

The integrated output voltage v_{out} is then converted to current by the VIC resistor, R_2 in Fig.4, when the other side of R_2 away from the opamp is connected to an virtual ground point. A virtual ground point is the input of an opamp where there is no AC voltage swing.

When the DCOC block is used as negative feedback with the signal path as shown in Fig.5, the high frequency (HF) components are filtered out by the LPF. Only dc and low frequency (LF) components remain after the LPF and are fed back to the signal path, in inverse polarity. The result is that the HF components are kept in the signal path, while the dc and LF components are removed

or largely attenuated from the signal spectrum, right after the summing point. The overall operation is thus a HPF function for the signal. For an ideal opamp in the integrator, the cutoff frequency is proportional to $R_4/(2\pi R_1 C_1 R_2)$.

The summing method chosen in present invention is input current summing. It is realized by summing the signal current and DCOC current at the input of an opamp in the signal path. The opamp can be in a filter internal stage, or in variable gain amplifier (VGA), or in BB driver. Fig.5 gives such an example. The operation can be interpreted as follows: If there is a DC offset inherent in the output voltage Vout of OPAMP2, it integrates through the integrator OPAMP1 and convert to current through VIC resistor R_2. This current then sums with the signal input current in reverse polarity. Thus at the output, the DC offset will reduce. The feedback loop bandwidth can be adjusted by the variable resistor R_1 in the integrator. This variable bandwidth can be used to adjust the cutoff frequency. The attenuation level at DC and LF is controlled by the bandwidth of the loop and the DC gain of the opamp in the integrator. The opamp in the integrator OPAMP1 must have large output swing, to maintain good linearity and effectively cancel DC offset. Besides, a larger swing can generate larger current through VIC resistor R_2. In another word, one can tolerate smaller integrating capacitor C_1 for fixed DC offset, or the same C_1 for larger DC offset, to save silicon area in design. In this invention, a rail-to-rail (full supply voltage) output opamp is used. Multiple DCOC circuits can be placed in the ZIF receiver, to form multiple DCOC blocks. Each block can involve or do not involve gain in signal path, depending on the particular system specification.

The input current summing method has a superior feature over the output current summing method as described in U.S. Pat. No. 6,509,777, or passive HPF AC coupler as described in U.S. Pat. No. 6,442,380, because it can save power or greatly reduce capacitor or resistor value in the integrator to achieve the same HPF transfer function. For comparison, assume ideal opamp in integrator and fixed integrating resistor value R_1. In an output current summing method as shown in Fig.2, the integrating voltage is added to a device input such as the gate of MOSFET or the base of BJT. The transconductance (gm) of the device then transfer the voltage into a current and summing it with the signal current which is amplified by the transconductance gm of another similar device in signal path at the output of the device. Generally, it needs more current to cancel the DC offset at output of the device than at the input of the device because the DC offset in signal at output of the device is amplified as well as the signal by the other device. Therefore, the gm of the DCOC device cannot be too small. Thus this method consumes more power than the input current summing

method. In a passive HPF method on the other hand, the HPF cut off frequency is defined as $f_c = 1/(2\pi RC)$. For the same f_c, the input current summing method has an integrating RC time constant that is proportional to R_2 / R_4 as shown in Fig.5. This can drastically reduce the integrating R or C value and thus the silicon area, by easily choosing $R_2 >> R_4$ in design.

A simulation result is provided in Fig.6. The simulation is based on a ZIF receiver BB 5th-order LPF with the DCOC block added to the output and input of the last opamp in the filter. The total gain of the LPF is set to 20dB. Four cutoff frequencies from 1KHz to 1MHz are achieved by adjusting variable resistor R_1. The parameters in this simulation are: $R_1 = 5M\Omega, 500K\Omega, 50K\Omega, 5K\Omega, C_1 = 7.5pF$, $R_2 = 20K\Omega$ $R_4 = 5K\Omega$. It is flexible to add the DCOC block in some other way, like adding it to the output of the last opamp and input of an internal opamp that is before the last opamp. To involve how many stages in signal path to the loop is an option of the designer according to his particular design.

While differential stages are used in the preferred embodiment of the BB amplifier as described in Fig.5, it will be obvious to those skilled in the art that the same technique can be used for single-ended stages. For instance, the opamp can have one non-inverting input grounded to effect a virtual ground at the inverting input, where the signal current and the feedback current are summed. Single-ended opamps can be used in the BB low pass stage, the BB VGA or the BB driver. Other modifications of the embodiment can be made without departing from the spirit of the present invention. Such modifications are all within the scope of the present invention.